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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/931,072	08/15/2001	Erik Cota-Robles	42390P10807	2890

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EXAMINER

BULLOCK JR, LEWIS ALEXANDER

ART UNIT	PAPER NUMBER
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2195

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/931,072

Applicant(s)

COTA-ROBLES ET AL.

Examiner

Lewis A. Bullock, Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 March 2005.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-36 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 15 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/14/04.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country; more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-36 are rejected under 35 U.S.C. 102(b) as being anticipated by MATSUURA (U.S. Patent 5,530,860).

As to claim 1, MATSUURA teaches a method comprising: trapping, by a processor, a change in execution among schedulable entities (virtual machines) (via sending an interruption when the virtual machine waits / time up for virtual machine) (col. 10, lines 12-20; col. 10, lines 47-63; col. 14, lines 12-22; fig. 12; col. 9, lines 60-67; col. 10, lines 1-30); and tracking an execution of a schedulable entity (virtual machine) that is being switched in for execution as a result of the change in execution (col. 10, lines 21-31).

As to claim 2, MATSUURA teaches the tracking is performed by a privilege entity (control program / virtual machine monitor / assignment order control unit) (col. 7, lines 46-55; col. 8, lines 23-41) and further comprising: calculating, by the privilege entity, an

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estimated resource requirement (priority detailing the CPU assignment ratio) for the schedulable entity (virtual machine) that is being switched in for execution from the tracking of a previous execution of the schedulable entity (virtual machine) (col. 8, lines 4-21; col. 8, lines 33-42; col. 8, line 60 – col. 9, line 18); and scheduling, by the privileged entity (control program / virtual machine monitor / assignment order control unit), the schedulable entity (virtual machine) that is being switched in for execution according to its estimated resource requirement (CPU assignment ratio) (col. 8, lines 4-21; col. 8, lines 33-42; col. 8, line 60 – col. 9, line 18).

As to claim 3, MATSUURA teaches the privilege entity is a virtual machine monitor (control program / virtual machine monitor / assignment order control unit) (col. 7, lines 46-55; col. 8, lines 23-41) and the schedulable entities are selected from the virtual machines (virtual machines) (fig. 9).

As to claim 4, MATSUURA teaches the virtual machine monitor (control program / virtual machine monitor / assignment order control unit) comprises: an idle detector to receive notice from the processor of the change in execution (via an interruption signal) and to derive a measured value for a schedulable entity that is being switched out of execution (via determining what part of time has passed, i.e. 10%) (col. 10, lines 11-30; col. 12, lines 29-43); a proportional integral derivative (PID) controller (control program / assignment order control unit) logically coupled to the idle detector to receive the measured value (part of time that has passed / 10%) and to calculate the estimated

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resource requirement (assignment ratio) required by the schedulable entity (virtual machine) that is being switched out of execution (via determining its new assignment ratio); and a scheduler logically coupled to the PID controller to receive the estimated resource requirement (new assignment ratio) and to determine a schedule of execution for the schedulable entity that is being switched out of execution (schedule in waiting queue until the virtual machine is operative and reassigned into operative queue based on assignment ratio and number of times operative) (col. 12, lines 29-59).

As to claim 5, MATSUURA teaches calculating an estimated resource requirement comprises: assigning an initial value as the estimated resource requirement (assigned ratio) for the schedulable entity (virtual machine) that is being switched in for execution; and increasing the estimated resource requirement for the schedulable entity if the schedulable entity does not complete execution before the estimated resource requirement is exhausted (via increasing the counter regarding the number of times operated) (col. 10, lines 1-10; col. 11, lines 44-62). MATSUURA also teaches that the assignment order control unit knows the operation state of the guest virtual machine only by the reception of interrupts wherein based on the interrupt it stores the remaining time in the column of assignment ratio (col. 9, line 60 – col. 10, line 20). It is inherent within the teachings of MATSUURA that if a virtual machine generates an interrupt notifying the processor of its completion within an assigned time, that the assigned ratio is reduced to zero.

As to claim 6, MATSUURA teaches initiating, by the privileged entity (virtual machine monitor / control program / assignment order control unit), the change in execution (via the activate instruction or a timer interrupt) (col. 9, lines 60 – col. 10, lines 10).

As to claim 7, MATSUURA teaches tracking of the execution is performed as part of the change in execution initiated by the privileged entity (virtual machine monitor / control program / assignment order control unit) (col. 9, lines 60 – col. 10, lines 10).

As to claim 8, MATSUURA teaches initiating, by the processor, the change in execution if the change in execution is being requested by the privileged entity (via executing a new virtual machine) (col. 9, lines 60 – col. 10, lines 10).

As to claim 9, MATSUURA teaches trapping a change in execution comprises: detecting an instruction to change a state register (assignment ratio / pointer information) that identifies a schedulable entity (virtual machine) (col. 8, lines 1-32).

As to claim 10, MATSUURA teaches comparing, by the processor, the state register (number of times of operation of a virtual machine value) that identifies the schedulable entity (virtual machine) being switched in for execution with a state match register (common number of times of operation value) that identifies a schedulable entity (virtual machine) that is to be tracked, wherein the schedulable entity being

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switched into execution is tracked by the processor if the state register and the state match register match (via determining that all guest virtual machines have been operated and therefore the current virtual machine can be switched in the subsequent CPU assignment cycle based on being the highest priority virtual machine) (col. 11, lines 44-63).

As to claim 11, MATSUURA teaches trapping a change in execution comprises: detecting an instruction to change between privileged (execution mode) and non-privileged modes (waiting / stopped mode) (via an interruption indicating that the virtual machine is waiting and not execution mode) (col. 10, lines 11-30).

As to claim 12, MATSUURA teaches the schedulable entities are virtual machines to be executed by the processor (fig. 9, 1).

As to claims 13-24, reference is made to a machine-readable medium that corresponds to the method of claims 1-12 and is therefore met by the rejection of claims 1-12 above.

As to claims 25-34, reference is made to an apparatus that corresponds to the method of claims 1-12 and is therefore met by the rejection of claims 1-12 above.

As to claims 35 and 36, refer to claims 10 and 12 for rejection.

3. Claims 1, 11-13, 23-25, and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by GEE (U.S. Patent 6,374,286).

As to claim 1, 11, 12, GEE teaches a method comprising: trapping, by a processor (JEM processor), a change in execution among schedulable entities (virtual machines) (via receiving a timer interruption regarding the virtual machine, i.e. the time for the virtual machine execution has ended); and tracking an execution of a schedulable entity that is being switched in for execution as a result of the change in execution (via context switching of virtual machines) (abstract; col. 25, lines 30-65) wherein the trapping comprises: detecting an instruction to change between privilege (executive mode) and non-privileged (user mode) modes (processor enters executive mode / processor enters user mode) (col. 26, lines 39-63) and the schedulable entities are operating system processes, virtual machines, or instruction streams to be executed by the processor (java processor) (col. 3, line 50 – col. 4, line 3; col. 19, lines 40-52).

As to claims 13, 23 and 24, reference is made to a machine-readable medium that corresponds to the method of claims 1, 11 and 12 and is therefore met by the rejection of claims 1, 11 and 12 above.

As to claims 25 and 31-34, reference is made to an apparatus that corresponds to the method of claims 1 and 11 and is therefore met by the rejection of claims 1 and 11 above.

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Response to Arguments

4. Applicant's arguments filed 3/2/05 have been fully considered but they are not persuasive. Applicant argued that the present invention teaches trapping by the processor a change in execution among schedulable entities wherein Matsuura's teaching performs the opposite such that the interrupt is not caused by a change in execution but a change in execution may result from the interrupt. The examiner disagrees. The cited claim language in question state "trapping, by a processor, a change in execution among schedulable entities". Interpretation of the limitation, means that the processor traps any change in execution from a schedulable entities. This would include if the schedulable entity is paused, stopped, crashed, and so forth, because these scenarios change the execution of the schedulable entity. Applicant's claims does not preclude this interpretation, therefore the claims have been interpreted as such. Matsuura teaches that the processor determines when a running time of the processor has passed and passes an interrupt to the control program (see col. 14, lines 12-22) or the step of detecting when a guest VM is waiting by sending interrupts to the control program for processing (see fig. 12; col. 9, lines 60-67; col. 10, lines 1-30). Therefore, since the processor sends to the interrupts when the virtual machine has used up its time or is waiting, it must inherently trap a change in execution among schedulable entities. Therefore, Matsuura does teach the limitation as disclosed.

Applicant argued that Gee does not teach the trapping a change in execution among schedulable entities. The examiner disagrees. For similar reasons as disclosed regarding Matsuura, the examiner disagrees with the arguments for in Gee. The cited

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claim language in question state "trapping, by a processor, a change in execution among schedulable entities". Interpretation of the limitation, means that the processor traps any change in execution from a schedulable entities. This would include if the schedulable entity is paused, stopped, crashed, and so forth including when a time period has expired for executing the virtual machine, because these scenarios change the execution of the schedulable entity. Applicant's claims does not preclude this interpretation, therefore the claims have been interpreted as such. As Applicant has stated, Gee teaches switching from a currently operating JVM to a master JVM at the end of a partition time period. These switches are performed based on interrupts. Gee states that a partition interrupt which is a non-maskable interrupt, occurs. The interrupt causes the JEM microcode in the processor to vector to an NMI interrupt handler which initializes the switching of the current JVM for another JVM (col. 25, lines 30-65). Again, because the limitation only requires the processor to trap a change in execution among schedulable entities, the processor receiving the timer interrupt to switch the execution of the virtual machines qualifies as meeting this limitation. Applicant's interpretation regarding the trapping of a context switch does not apply because the interpretation of a change in execution is not limited to a context switch. Therefore, Gee does teach the limitation as disclosed.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

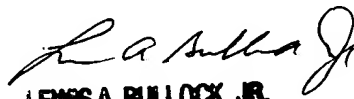
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 13, 2005


LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER